WHAT IS CLAIMED IS:

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1. An apparatus comprising:

a first conductivity type junction formed between a first region of a first conductivity type and a second region of a second conductivity type;

a second conductivity type junction formed between the second region and a third region of the first conductivity type;

a third conductivity type junction formed between the third region and a fourth region of the second conductivity type, wherein the first, second and third conductivity type junctions are associated with a thyristor; and

a low voltage trigger control coupled to the second region and the third region to provide a thyrister triggering current at a voltage of less than 10 volts.

2. The apparatus of claim 1, further comprising:

a first voltage reference node coupled to the first conductivity type junction;

a second voltage reference node adapted to be isolated from the first voltage reference node during normal operating conditions, coupled to the fourth conductivity type junction to provide a current path between the first voltage reference node and the second voltage reference node during an electrostatic event.

3. The apparatus of claim 2, wherein the first voltage reference node and the second voltage reference node are ground nodes.

4. The apparatus of claim 1, wherein a capacitance between the first region and the fourth region is less than 120 fentofarads.

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5. The apparatus of claim 4 having a conductance between the first region and the fourth region of greater than 0.5 mhos when in an on state during an electrostatic discharge event.

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6. The apparatus of claim 1 having a conductance between the first region and the fourth region of greater than 0.5 mhos when in an on state during an electrostatic discharge event.

7. The apparatus of claim 1, wherein the low voltage trigger includes a zener diode.

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8. The apparatus of claim 7, further comprising:

a first voltage reference node coupled to the first the first conductivity type junction;

a second voltage reference node adapted to be isolated from the first voltage reference node during normal operating conditions, coupled to the fourth conductivity type junction to provide a current path between the first voltage reference node and the second voltage reference node during an electrostatic event.

9. The apparatus of claim 7, wherein the zener diode includes a fifth region of the first conductivity type formed at least partially overlying the third region, and the fifth region has a different amount of doping than the third region.

10. The apparatus of claim 9, wherein the zener diode further includes a sixth region of the second conductivity type formed overlying the fifth region and the second region

11. The apparatus of claim 1, wherein the low voltage trigger includes a field effect transistor.

12. The apparatus of claim 11, wherein the field effect transistor includes a first current node coupled to the second region, a second current node coupled to the fourth region, and a control node coupled to the second region.

13. The apparatus of claim 11, further comprising:

a first voltage reference node coupled to the first conductivity type junction; and

a second voltage reference node adapted to be isolated from the first voltage reference node during normal operating conditions, coupled to the fourth conductivity type junction to provide a current path between the first voltage reference node and the second voltage reference node during an electrostatic event.

14. The apparatus of claim 13, wherein the control node includes a gate structure formed over a portion of the third region.

15. The apparatus of claim 14, wherein the first node is connected to a fifth region of the second conductivity type formed overlying the second region and the third region.

16. The apparatus of claim 14, wherein the gate structure is formed over an area between the fifth region and the fourth region.

17. The apparatus of claim 1 wherein the apparatus is formed using a complimentary metal oxide semiconductor process.

18. A thyristor formed in an integrated data processing device, the thyristor comprising:
    a first conductivity type junction formed between a first region of a first conductivity type and a second region of a second conductivity type;
    a second conductivity type junction formed between the second region and a third region of the first conductivity type;
    a third conductivity type junction formed between the third region and a fourth region of the second conductivity type; and
    an anode node connected to one or more regions including the first region, wherein each of the one or more regions connected to the anode node are of a common connectivity type.

19. The thyrister of claim 18 further comprising:
    a low voltage trigger control portion coupled to the second region and the third region to provide a thyrister triggering current at a voltage of less than 10 volts.

20. The thyristor of claim 18 formed using a complimentary metal oxide semiconductor process.

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21. An apparatus comprising:

a first voltage reference node to provide a first voltage reference;

a second voltage reference node, adapted to be isolated from the first voltage reference node during normal operating conditions, to provide the first voltage reference;

a thyristor coupled between the first voltage reference node and the second voltage reference node to provide a current path between the first voltage reference node and the second voltage reference node during an electrostatic event.

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23. The apparatus of claim 21 further comprising:

a first circuit connected to the first voltage reference node; and

a second circuit connected to the second voltage reference node.

24. The apparatus of claim 23, wherein the first circuit is an analog circuit and the second circuit is a digital circuit.

25. The apparatus of claim 23, wherein the first circuit is a radio frequency analog circuit.

26. The apparatus of claim 24, wherein the second circuit is a digital circuit.

27. The apparatus of claim 25, wherein the second circuit is an analog circuit.

28. A method comprising the steps of:

detecting a voltage difference between a first voltage reference node and a second voltage reference node to determine when an electrostatic discharge event is occurring;

providing conductive path through a thyrister when the voltage difference is less than approximately 10 volts.

29. The method of claim 28, wherein the first voltage reference node and the second voltage reference node are at a common potential during a normal mode of operation.